**i2si.v Document – Zachary Nelson**

**Interfaces:**

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Bits | Comment |
| clk | in | 1 | Master Clock |
| rst | in | 1 | Reset |
| i2si\_sck | in | 1 | Digital Audio Bit Clock (max of 48kHz) |
| i2si\_ws | in | 1 | Word Select (Left/Right Audio Channel) |
| i2si\_sd | in | 1 | Digital Audio Serial Data |
| i2si\_rtr | in | 1 | Ready to Receive |
| i2si\_rts | out | 1 | Ready to Send |
| i2si\_en | in | 1 | i2s input is enabled |
| ro\_fifo\_overrrun | out | 1 | Input Audio FIFO Overrun |
| rf\_bist\_en | in | 1 | Built in Self-Test (BIST) |
| i2si\_lft | out | 16 | Left Parallel Digital Audio |
| i2si\_rgt | out | 16 | Right Parallel Digital Audio |

**Functional Requirements:**

* Data Plane Requirements:
  + If the rf\_bist\_en control bit is true, the output of the block will be pre-defined such as a fixed sawtooth wave. If not, the input audio data will be pushed into the FIFO buffer and popped. The block will also need to convert audio serial data into 16-bit digital audio.
* Control Plane Requirements:
  + Serial data is transmitted in two’s complement with the Most Significant Bit (MSB) first. Serial data must be latched into the receiver on the leading edge of the serial clock signal. See Section 3.1 of I2S Specification Sheet for more details.
  + Support audio input sample rates of 8 kilosamples/sec – 48 kilosamples/sec.
  + The buffer sizing will have 2 or 3 storage elements which means we need a pointer that is 2 bits.
  + Overflow is a possibility because the FIFO buffer could be full when trying to input audio. In this case, the input will be ignored and the buffer will not change.
* Control and Status Interface Bit Descriptions:
  + Control Bits
    - i2si\_ws: selects w­hat audio channel is being read. 0 = left channel, 1= right channel.
    - i2si\_in\_en: i2s input is enabled
    - rf\_bist\_en: built in self-test
  + Status Bits
    - ro\_fifo\_overrun: The FIFO buffer is full and no more can be added to the buffer
    - i2si\_rtr: Output FIFO asserts ready to receive
    - i2si\_rts: Write Client asserts ready to send

**Micro-Architecture:**

* Sub-blocks
  + i2si\_bist\_gen.v

|  |  |  |
| --- | --- | --- |
| Signal Name | Bits | Comment |
| rf\_bist\_start\_val | 16 | start value |
| rf\_bist\_inc | 8 | increment |
| rf\_bist\_upper\_limit | 16 | upper limit |

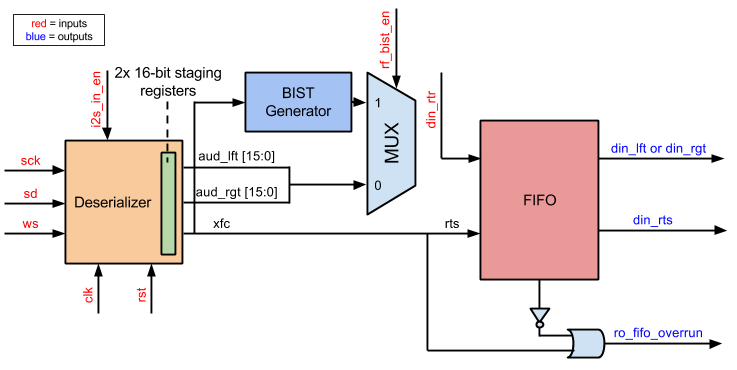
* + i2si\_fifo.v

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Bits | Comment |
| clk | in | 1 | Master Clock |
| rst | in | 1 | Reset |
| i2si\_fifo\_inp\_data | in | 16 | Input Data |
| i2si\_fifo\_inp\_rts | in | 1 | Write Client Asserts Ready to Send |
| i2si\_fifo\_inp\_rtr | out | 1 | Output FIFO Asserts Read to Receive |
| i2si\_fifo\_out\_data | out | 16 | Output FIFO Asserts Ready to Send |
| i2si\_fifo\_out\_rts | out | 1 | Output FIFO Asserts Ready to Send |
| i2si\_fifo\_out\_rtr | in | 1 | Read Client Asserts Read to Receive |

* + i2si\_deserialzier.v

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Bits | Comment |
| clk | in | 1 | Master Clock |
| rst | in | 1 | Reset |

* Block Diagram



**Design:**

**Verification:**